



Application No. 10/002,176
Amendment dated September 27, 2006
First Preliminary Amendment

Docket No.: M4065.0210/P210-A

AMENDMENTS TO THE CLAIMS

Claims 1-31 (Canceled).

32. (Currently amended) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom conducting layer, wherein said bottom conducting layer forms a bottom electrode;

forming a dielectric layer over the bottom conducting layer, and annealing said dielectric layer with a first anneal process;

forming a top electrode with a top conducting layer over the annealed dielectric layer, wherein said top conducting layer is formed of a material selected from the group consisting of Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium Oxide (RuO₂), Rhodium Oxide (RhO₂), Chromium Oxide (CrO₂), Molybdenum Oxide (MoO₂), Rhodium Oxide (ReO₃), Iridium Oxide (IrO₂), Titanium Oxides (TiO₁ or TiO₂), Vanadium Oxides (VO₁ or VO₂), and Niobium Oxides (NbO₁ or NbO₂); and

annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes ~~at a pressure less than 760 Torr.~~

33. (Original) A method of forming a capacitor of claim 32, wherein said capacitor is formed over a conductive plug, said method further comprising depositing an oxygen barrier over said conductive plug prior to forming the bottom conducting layer.

34. (Original) A method of forming a capacitor of claim 32, said method further comprising: annealing the dielectric layer after it is formed.

35. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the noble metal group.

36. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal.

37. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal alloy.

38. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a conducting metal oxide.

39. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a metal nitride.

40. (Original) A method of forming a capacitor of claim 32, wherein said bottom conducting layer is formed of a material selected from the group consisting of: Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium, Ruthenium Oxide (RuO₂), Rhodium Oxide (RhO₂), Chromium Oxide (CrO₂), Molybdenum Oxide (MoO₂), Rhodium Oxide (ReO₃), Iridium Oxide (IrO₂), Titanium Oxides (TiO₁ or TiO₂), Vanadium Oxides (VO₁ or VO₂), Niobium Oxides (NbO₁ or NbO₂), and Tungsten Nitride (WN_x, WN or W₂N).

41. (Original) A method of forming a capacitor of claim 40, wherein said bottom conducting layer is formed of a material selected from the group consisting of:

Platinum (Pt), Platinum Rhodium (PtRh), Platinum Iridium (PtIr), and Tungsten Nitride (WN_x, WN or W₂N).

42. (Original) A method of forming a capacitor of claim 32, wherein said dielectric layer is a dielectric metal oxide layer.

43. (Original) A method of forming a capacitor of claim 32, wherein said dielectric layer has a dielectric constant between 7 and 300.

44. (Original) A method of forming a capacitor of claim 32, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta₂O₅), Barium Strontium Titanate (BST), Aluminum Oxide (Al₂O₃), Zirconium Oxide (ZrO₂), Praseodymium Oxide (PrO₂), Tungsten Oxide (WO₃), Niobium Pentoxide (Nb₂O₅), Strontium Bismuth Tantalate (SBT), Hafnium Oxide (HfO₂), Hafnium Silicate, Lanthanum Oxide (La₂O₃), Yttrium Oxide (Y₂O₃), and Zirconium Silicate.

45. (Original) A method of forming a capacitor of claim 44, wherein said dielectric layer is formed of a material selected from the group consisting of: Tantalum Oxide, Tantalum Pentoxide (Ta₂O₅), Barium Strontium Titanate (BST), Strontium Bismuth Tantalate (SBT), Aluminum Oxide (Al₂O₃), Zirconium Oxide (ZrO₂) and Hafnium Oxide (HfO₂).

46. (Original) A method of forming a capacitor of claim 45, wherein said dielectric layer is Tantalum Oxide and is crystalline or amorphous material.

47. (Previously presented) A method of forming a capacitor of claim 45, wherein said dielectric layer is an amorphous dielectric layer which is heated to a

temperature above 200 degrees Celsius to change said dielectric layer from an amorphous material to a crystalline material.

48. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a material selected from the noble metal group.

49. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a non-oxidizing metal permeable to oxygen:

50. (Original) A method of forming a capacitor of claim 32, wherein said top conducting layer is formed of a conducting metal oxide.

51. (Canceled)

52. (Currently amended) A method of forming a capacitor of claim 51, wherein said top conducting layer is formed of a material selected from the group consisting of: ~~Platinum (Pt)~~, Platinum Rhodium (PtRh), and Platinum Iridium (PtIr).

53. (Currently amended) A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: ~~Platinum~~, Platinum Rhodium (PtRh), or Platinum Indium (PtIr) and said dielectric layer is a layer of Tantalum Oxide.

54. (Currently amended) A method of forming a capacitor of claim 32, wherein said bottom and top conducting layers are formed of a material selected from the group consisting of: ~~Platinum~~, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and said dielectric layer is a layer of Barium Strontium Titanate (BST) or Strontium Bismuth Tantalate (SBT).

55. (Currently amended) A method of forming a capacitor of claim 32, wherein said top conducting layers are formed of a material selected from the group consisting of ~~Platinum~~, Platinum Rhodium (PtRh), or Platinum Iridium (PtIr) and, said bottom conducting layer is a layer of Tungsten Nitride (WN_x, WN or W₂N) layer, and said dielectric layer is a layer of Aluminum Oxide (Al₂O₃).

56. (Canceled).

57. (Previously presented) A method of forming a capacitor of claim 32, wherein said annealing is performed with a material selected from the group consisting of: Oxygen (O₂), Ozone (O₃), Nitrous Oxide (N₂O), Nitric Oxide (NO), and water vapor (H₂O).

58. (Original) A method of forming a capacitor of claim 57, wherein said annealing is performed with a gas mixture containing at least one element selected from the group consisting: Oxygen (O₂), Ozone (O₃), Nitrous Oxide (N₂O), Nitric Oxide (NO), and water vapor (H₂O).

59. (Previously presented) A method of forming a capacitor of claim 32, wherein said annealing is a plasma enhanced annealing.

60. (Original) A method of forming a capacitor of claim 59, wherein said annealing is a remote plasma enhanced annealing.

61. (Previously presented) A method of forming a capacitor of claim 32, wherein said annealing is an ultraviolet light enhanced annealing.

62. (Original) A method of forming a capacitor of claim 32, wherein said annealing is performed at a temperature between 300 and 800 degrees Celsius.

63. (Original) A method of forming a capacitor of claim 62, wherein said annealing is performed at a temperature between 400 and 750 degrees Celsius.

64. (Canceled).

65. (Original) A method of forming a capacitor of claim 64, wherein said annealing is performed at a pressure between 2 and 660 Torr.

Claims 66-67 (Canceled).

68. (Previously presented) A method of forming a capacitor of claim 32, wherein said annealing is performed in the presence of an oxygen gas with a flow rate between 0.01 and 10 liters per second.

Claims 69-96 (Canceled).

97. (Currently amended) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom electrode;

forming a dielectric layer over the bottom electrode;

forming a top electrode over said dielectric layer; and

annealing said top electrode with an oxidizing gas anneal at a temperature greater than 400°C ~~and a pressure of less than 760 Torr.~~

98. (Currently amended) A method of forming a capacitor in a semiconductor device, said method comprising:

forming a bottom electrode;

forming a dielectric layer over the bottom electrode;

annealing the dielectric layer with a first oxidizing gas anneal for about 10 seconds to about 60 minutes, at a temperature from about 300 to about 800°C, ~~and at a pressure of less than 760 Torr~~;

forming a top electrode over said annealed dielectric layer; and annealing said top electrode with a second oxidizing gas anneal for about 10 seconds to about 60 minutes, at a temperature from about 300 to about 800°C, ~~and at a pressure of less than 760 Torr~~.